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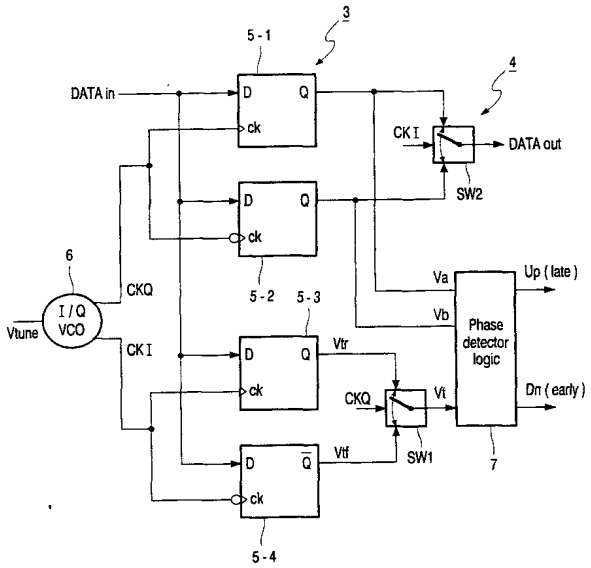
(54) Title: DATA CLOCKED RECOVERY CIRCUIT



(57) Abstract: A data clock recovery circuit (3) comprises a controllable quadrature clock oscillator (6) operating at half the data rate of data input to said circuit, and a phase detector logic (7) having detector inputs coupled to the data input and having a detector output coupled to a frequency control input of the quadrature clock oscillator. The data clock recovery circuit further comprises a parallel arrangement of sampling devices, (5-1, 5-2, 5-3, 5-4) in particular flip-flops each having a clock input (CR) which is coupled to the controllable quadrature clock oscillator, a data input for the data input (D) to said circuit, and a data output coupled to the phase detector. Accurate control of the phase of recovered data is possible with the present circuit, which is easy to integrate on a limited chip area and in a low power consuming way.

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DATA CLOCKED RECOVERY CIRCUIT

The present invention relates to a data clock recovery circuit comprising a controllable quadrature clock oscillator operating at half the data rate of data input circuit, and a phase detector logic having detector inputs coupled to the data input and having a detector output coupled to a frequency control input of the quadrature clock oscillator.

The present invention also relates to a data receiver provided with such a data clock recovery circuit and to a communication device, such as an optical communication device provided with such a data clock recovery circuit.

Such a clock recovery circuit is known from US-A-5,301,196. The known clock recovery circuit is provided with a controllable quadrature clock oscillator, a phase detector logic in the form of a phase comparator having comparator data inputs coupled to I and Q outputs of the quadrature oscillator and having comparator clock inputs coupled to a data input of the clock recovery circuit. The known clock recovery circuit is provided with a loop filter interconnecting a data output of the phase comparator and a control input of the controllable quadrature clock oscillator. The clock recovery circuit generates quadrature oscillator signals at half the rate of data input stream received on a data input of the recovery circuit. The quadrature oscillator signals are sampled by the input data in sampling devices, embodied as edge triggered flip-flops and then XORed to provide a loop filter signal. In addition the recovery circuit comprises a demultiplexer circuit. This demultiplexer circuit comprises a parallel arrangement of sampling devices in the form of flip-flops, each having a clock input which is coupled to the controllable quadrature clock oscillator, a data input for the data input to said recovery circuit, and a demultiplexer output for providing demultiplexed data. The demultiplexer circuit uses the rising and falling edges of the half speed quadrature clock to latch the input data stream through the pair of flip-flops.

It is a disadvantage of the known clock recovery circuit that cumulative delays arise, which are caused by the flip-flops, the XOR, the loop filter and the ring oscillator respectively. These delays in addition to delays caused by necessary run time delay data of the oscillator loop lead to a low accuracy and to decision errors in the recovered data.

It is an object of the present invention to provide an improved data clock recovery circuit, which may be fully integrated on a limited chip area and which shows an improved accuracy and robustness.

Thereto the data clock recovery circuit according to the invention is characterized in that the data clock recovery circuit further comprises a parallel arrangement of sampling devices each having a clock input which is coupled to the controllable quadrature clock oscillator, a data input for the data input to said circuit, and a data output coupled to the phase detector logic.

It is an advantage of the data clock recovery circuit according to the present invention that in the recovery circuit the quadrature oscillator signal is used a as clock signal for clocking the data input stream. Because the data input stream is thus clocked as recovered data to the phase detector logic this logic is capable of providing tight control over the thus improved phase accuracy of the recovered data. Furthermore the data clock recovery circuit according to the invention is self-correcting which means that the time delays at the place of the data output are controlled away, which means that decision errors in the recovered bits are reduced.

An easy to integrate embodiment of the data clock recovery circuit according to the invention is characterized in that the sampling devices form a parallel arrangement of flip-flops. These flip-flops are in a further embodiment provided with clock inputs which are responsive to either the raising, or falling edges of the respective I and Q oscillator signals of the quadrature clock oscillator. In this case the flip-flops are easy to manufacture D or edge flip-flops.

A further embodiment of the data clock recovery circuit according to the invention is characterized in that the data outputs of the respective sampling devices are coupled to controllable switches each having a switch control input coupled to the quadrature clock oscillator, two data inputs coupled to the respective outputs of the sampling devices, and switch outputs for providing serial output data.

Although in certain practical implementations of the present invention it may be useful to directly use the recovered/regenerated parallel data output stream from the parallel arrangement of sampling devices, it may in other implementations be more useful to multiplex the parallel data output stream to a serial output data stream. The latter data stream is now generated by a simple multiplexer in the form of controllable switch.

A still further embodiment of the data clock recovery circuit according to the invention is characterized in that one of the controllable switches is replaced by a latch device, the latch device having a clock input coupled to the quadrature clock oscillator, and a data input coupled to the respective output of the sampling device.

Advantageously the embodiment having a latch device provides a latch data output signal having transitions arising a the same time as transitions at the corresponding output of the respective sampling device.

Another embodiment of the data clock recovery circuit according to the invention is characterized in that said circuit comprises (bit error rate) BER detector logic, and the data outputs of the respective sampling devices are coupled to a further controllable switch having a switch control input coupled to the quadrature clock oscillator, two data inputs coupled to the respective outputs of the sampling devices, and a switch output coupled to the BER detector logic.

Advantageously the fully to integrate and thus low power consuming present embodiment is capable of providing bit error rate information, which may be used for error indication and/or correction purposes. The additional chip area necessary to implement this function is advantageously small.

Still another easy to implement embodiment of the data clock recovery circuit according to the invention is characterized in that the phase detector logic and the bit error rate detector logic comprise elementary digital logic circuits, such as exclusive OR gates, inverters and logic gates, like AND, NAND, OR, NOR gates.

At present the data clock recovery circuit, data receiver and communication device according to the invention will be elucidated further together with its additional advantages while reference is being made to the appended drawing, wherein similar components are being referred to by means of the same reference numerals.

In the drawing:

Fig. 1 shows a schematic representation of a data receiver for application in a communication device according to the invention;

Fig. 2 shows an outline of several possible embodiments of the data clock recovery circuit for application in the data receiver according to fig. 1;

Fig. 3 shows an illustration of signals for elucidating the operation of the data clock recovery circuit of fig. 2;

Fig. 6 shows a truth table for describing the operation of the of the phase detector logic for application in the data recovery clock circuit of fig. 3;

Fig. 4 shows several combined embodiments of the data clock recovery circuit in a demultiplexer configuration having a bit error rate detector logic, and

Figs. 5a and 5b show embodiments of phase detector logic and bit error rate logic respectively for application in the recovery circuits of figs. 2 and 4.

Fig. 1 shows a schematic representation of a data receiver 1 for application in a communication device, such a long-distance optical glass fibre communication device (not shown) SDH/SONET, or computer network, such as gigabit Ethernet. As shown a limiter 2 precedes the data receiver 1. Data is input to the limiter. The data receiver 1 comprises a data clock recovery circuit 3 and may comprise a demultiplexer 4. The data and clock recovered from the circuit 3 are fed to the demultiplexer 4, which provides a parallel data output. In particular serial input data, such as non-return-to-zero data is received and converted to recovered and synchronized parallel output data.

Fig. 2 shows an outline of several possible embodiments of the data clock recovery circuit 3 with or without serialiser 4, which circuit 3 is for application in the data receiver 1 of to fig. 1. Data input to the recovery circuit 3 at DATA in is fed to a parallel arrangement 5 of sampling devices 5-1, 5-2, 5-3 and 5-4 each having a clock input ck, a data input D coupled to DATA in, and a data output Q, Q invert. The sampling devices 5 may be flip-flops, such as D flip-flops. The recovery circuit 3 comprises a controllable quadrature clock oscillator 6 and a phase detector logic 7. The clock inputs ck of the sampling devices 5-1, 5-2 is coupled to the one quadrature output CKQ of the oscillator 6, while the other quadrature output CKI is coupled to clock inputs ck of the oscillator 6. Outputs Q of sampling devices 5-1, 5-2 provide parallel output data fed as Va and Vb to inputs of the phase detector logic 7. In a possible embodiment output signal Vtr of sampling device 5-3 can be coupled directly to input Vt of the detector logic 7. The logic 7 provides an UP/DN control signal for tuning the frequency of the quadrature oscillator signals CKQ and CKI by means of a frequency control input Vtune of the oscillator 6. In the embodiment as shown in fig. 2 the recovery circuit 3 comprises a controllable switch SW1 having a switch control input coupled to the signal CKQ and a controllable switch SW2 having a switch control input coupled to the signal CKI. Each of the controllable switches SW1 and SW2 have two data inputs coupled to the respective outputs Vtr, Vtf and Q, Q of devices 5-1, 5-2 respectively,

and switch outputs Vt and DATAout respectively for providing a further detector logic input signal and serialized output data respectively. The two switches SW1 and SW2 may be identical and there operation (related to SW1) is governed by the relations:

If CKQ=high then Vt=Vtr , if CKQ=low then Vt=Vtf.

If switch SW2, which functions as a multiplexer/serialiser is absent parallel output data is provided by the demultiplexing sampling devices 5-1, 5-2, else DATAout provides serial output data. By way of example the operation of the data clock recovery circuit 3 in the embodiment as fully shown in fig. 2 will be explained.

Fig. 3 shows an illustration of signals in consecutive intervals 1, 2,...5 for elucidating the operation of the data clock recovery circuit of fig. 2. Schematically it is illustrated in fig. 2, that the data input stream Din is sampled by the sampling circuits 5-1 and 5-3 at the rising edge of CKQ and CKI respectively, while sampling circuits 5-2 and 5-4 are sampled at the falling edge of clock signals CKQ and CKI respectively. Both the quadrature clock signals are exact copies of a 10101010 Din sequence, and thus after synchronization of the quadrature oscillator control loop these clock signals have a frequency which is half the bit-rate used. After synchronization has been accomplished, transitions in the DATAout signal will occur (ideally) at the rising and/or falling edges of the CKI signal. Therefore the CKQ signal, which is delayed by 90 degrees relative to the CKI signal can be used to sample the DATAin signal in the middle of the well known eye-diagram, which is the ideal moment therefor. This takes place in sampling circuits 5-1 and 5-2. Given an arbitrary Din pattern, in intervals 1 and 2 respectively the Din transitions lag the CKI transitions. The phase detector logic processes this in the next intervals 2 and 3 respectively setting the Dn signal active, which lowers the oscillator 6 frequency. Contrary in interval 4 Din transition precedes CKI transition, which is processed in interval 5 setting UP active, advancing the quadrature clock signals CKI and CKQ in phase. It is to be noted that in order to provide correct functionality in this case, with only one switch SW1, the inverted output Q invert has to provide the signal Vtf. The basic idea of the algorithm is that the Vt signal, which is derived from the samples taken during the rising and falling edges of CKI, will equal Vb when CKI transitions are leading the DATA in transitions, and will equal Va when CKI transitions are lagging the DATA in transitions.

During interval 3 no transitions are present in the DATA in signal and thus the Va and Vb signals are equal in the next interval. In that case, either the UP Dn signals are reset, or one of these signals may stay in the active state, as set by the information derived from the latest data transition. The former is a robust option to be used with unencoded data

signals, such as those employed in SDH/SONET networks, where very long sequences of 1's and 0's may occur. Correction signals are then only generated after transitions in the data are detected, and such correction signals do not last longer than one bit period. The latter option can only be applied in systems where the data is properly encoded so that a DC free content and minimum amount of transitions is guaranteed. The considerations of the foregoing lead to the truth Fig. 6.

Fig. 4 shows combined embodiments of the data clock recovery circuit 3 in a demultiplexer configuration having a bit error rate detector logic 8. SW2 of fig. 2 is replaced here by a D latch device 9, whose function is to synchronize the transitions of output signal b0 to the falling edge of CKQ. The D latch has a clock input ck coupled to the quadrature clock oscillator signal CKQ, and a data input D coupled to the respective output Q of the sampling device 5-1. By doing this both parallel outputs b0 and b1 have simultaneously occurring transitions. This architecture enables assessment of the data signal quality by enabling an estimation of the bit-error-rate (BER). Thereto the circuit 3 may further comprises a controllable switch SW3 having a switch control input CKQ coupled to the quadrature clock oscillator 6, two data inputs coupled to the respective outputs Q and Q of the sampling devices 5-3 and 5-4 respectively, and a switch output Vc coupled to the BER detector logic 8. Further BER detector inputs are formed by Va and Vb.

The functioning of the BER detector logic 8 is as follows. The value of the Va, Vb and Vc samples is compared, in case the condition Va equals Vb is fulfilled. As this means that no transition has taken place during the previous interval the Vc signals is expected to have the same value as Va and Vb. If this is not the case then the explanation is that a wrong decision has been taken by one or several of the sampling devices 5. This can only be explained by the presence of additive noise on the input data signal, leading to the conclusion that a degradation in the quality of the transmission channel has occurred, resulting in a BER related loss of signal.

Figs. 5a and 5b show embodiments of phase detector logic and bit error rate logic respectively for application in the recovery circuits of figs. 2 and 4. The very simple logic implementations exemplified here each comprise two exclusive OR circuits 9-1 to 9-4 whereto signals as indicated are fed. Logics 7 and 8 further comprise AND gates 10-1 to 10-3 for providing the UP/Dn signals and a BER flag for tuning the frequency of the quadrature oscillator 6 and for indicating an observed bit error respectively.

Whilst the above has been described with reference to essentially preferred embodiments and best possible modes it will be understood that these embodiments are by no

means to be construed as limiting examples of the devices concerned, because various modifications, features and combination of features falling within the scope of the appended claims are now within reach of the skilled person.

CLAIMS:

1. A data clock recovery circuit comprising a controllable quadrature clock oscillator operating at half the data rate of data input to said circuit, and a phase detector logic having detector inputs coupled to the data input and having a detector output coupled to a frequency control input of the quadrature clock oscillator, characterized in that the data clock recovery circuit further comprises a parallel arrangement of sampling devices each having a clock input which is coupled to the controllable quadrature clock oscillator, a data input for the data input to said circuit, and a data output coupled to the phase detector.

2. The data clock recovery circuit of claim 1, characterized in that the sampling devices form a parallel arrangement of flip-flops.

3. The data clock recovery circuit of claim 2, characterized in that the flip-flops are provided with clock inputs which are responsive to either the raising, or falling edges of the respective I and Q oscillator signals of the quadrature clock oscillator.

4. The data clock recovery circuit according to one of the claims 1-3, characterized in that the data outputs of the respective sampling devices are coupled to controllable switches each having a switch control input coupled to the quadrature clock oscillator, two data inputs coupled to the respective outputs of the sampling devices, and switch outputs for providing serial output data.

5. The data clock recovery circuit according to claim 4, characterized in that one of the controllable switches is replaced by a latch device, the latch device having a clock input coupled to the quadrature clock oscillator, and a data input coupled to the respective output of the sampling device.

6. The data clock recovery circuit according to claim 4 or 5, characterized in that said circuit comprises (bit error rate) BER detector logic, and the data outputs of the respective sampling devices are coupled to a further controllable switch having a switch

control input coupled to the quadrature clock oscillator, two data inputs coupled to the respective outputs of the sampling devices, and a switch output coupled to the BER detector logic.

7. The data clock recovery circuit according to one of the claims 1-6, characterized in that the phase detector logic and the bit error rate detector logic comprise elementary digital logic circuits, such as exclusive OR gates, inverters and logic gates, like AND, NAND, OR, NOR gates.

8. A data receiver provided with a data clock recovery circuit according to one of the claims 1-7, characterized in that the data clock recovery circuit further comprises a parallel arrangement of sampling devices each having a clock input which is coupled to the controllable quadrature clock oscillator, a data input for the data input to said circuit, and a data output coupled to the phase detector.

9. A communication device, such as an optical communication device provided with a data receiver according to claim 8, characterized in that the data clock recovery circuit further comprises a parallel arrangement of sampling devices each having a clock input which is coupled to the controllable quadrature clock oscillator, a data input for the data input to said circuit, and a data output coupled to the phase detector.

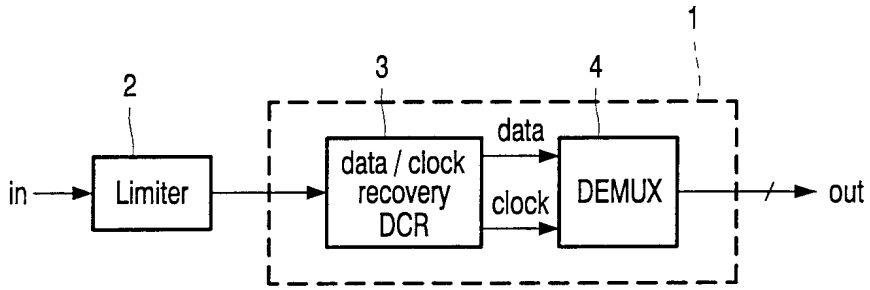
1
2
3
4
in
Limiter
data / clock recovery DCR
data
clock
DEMUX
out

FIG. 1

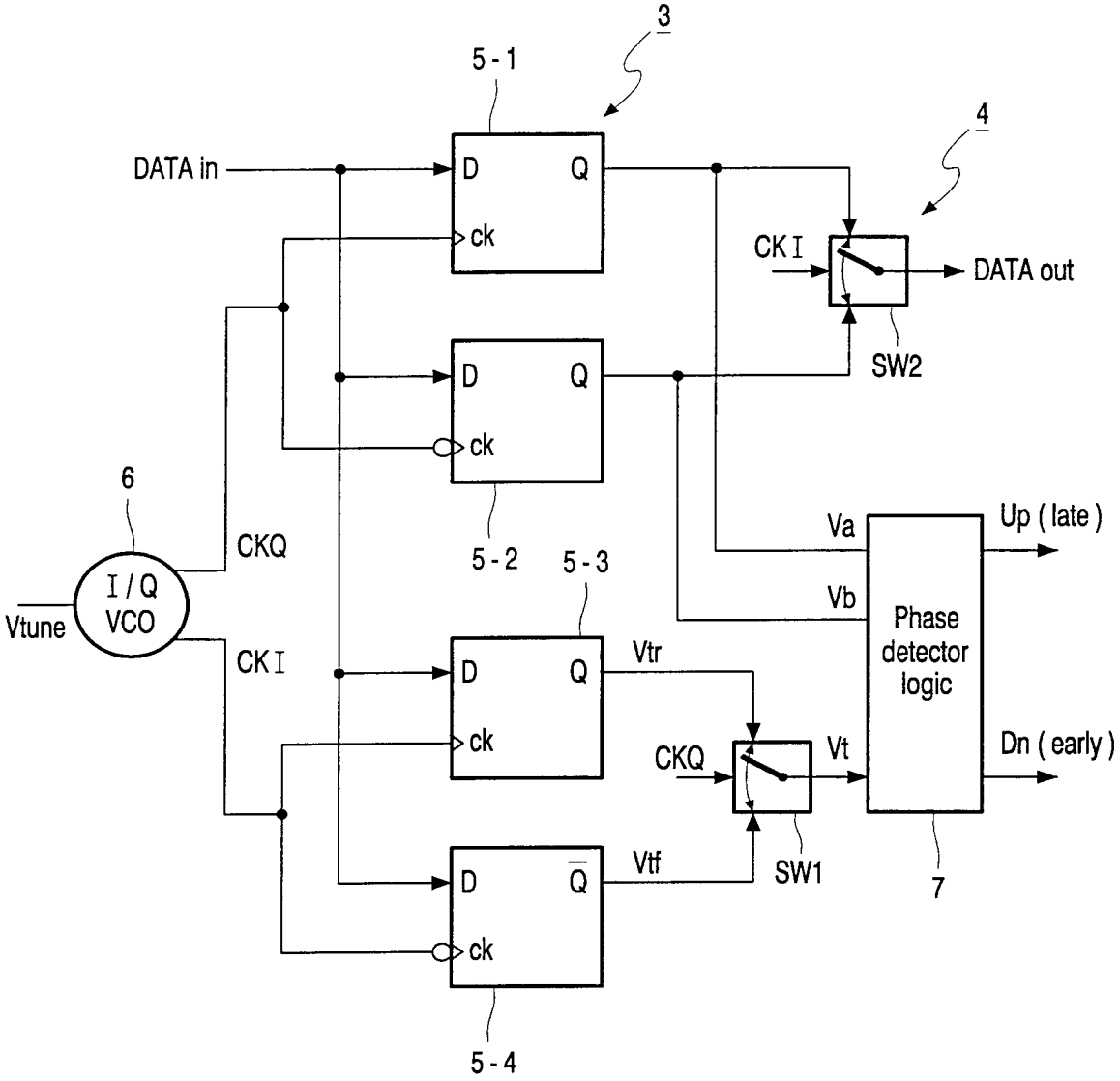
3
5 - 1
4
DATA in
D
Q
ck
CK I
DATA out
SW2
5 - 2
5 - 3
6
CKQ
I / Q VCO
Vtune
CK I
Va
Vb
Up (late)
Phase detector logic
Vtr
CKQ
Vt
Dn (early)
Vtf
SW1
7
5 - 4

FIG. 2

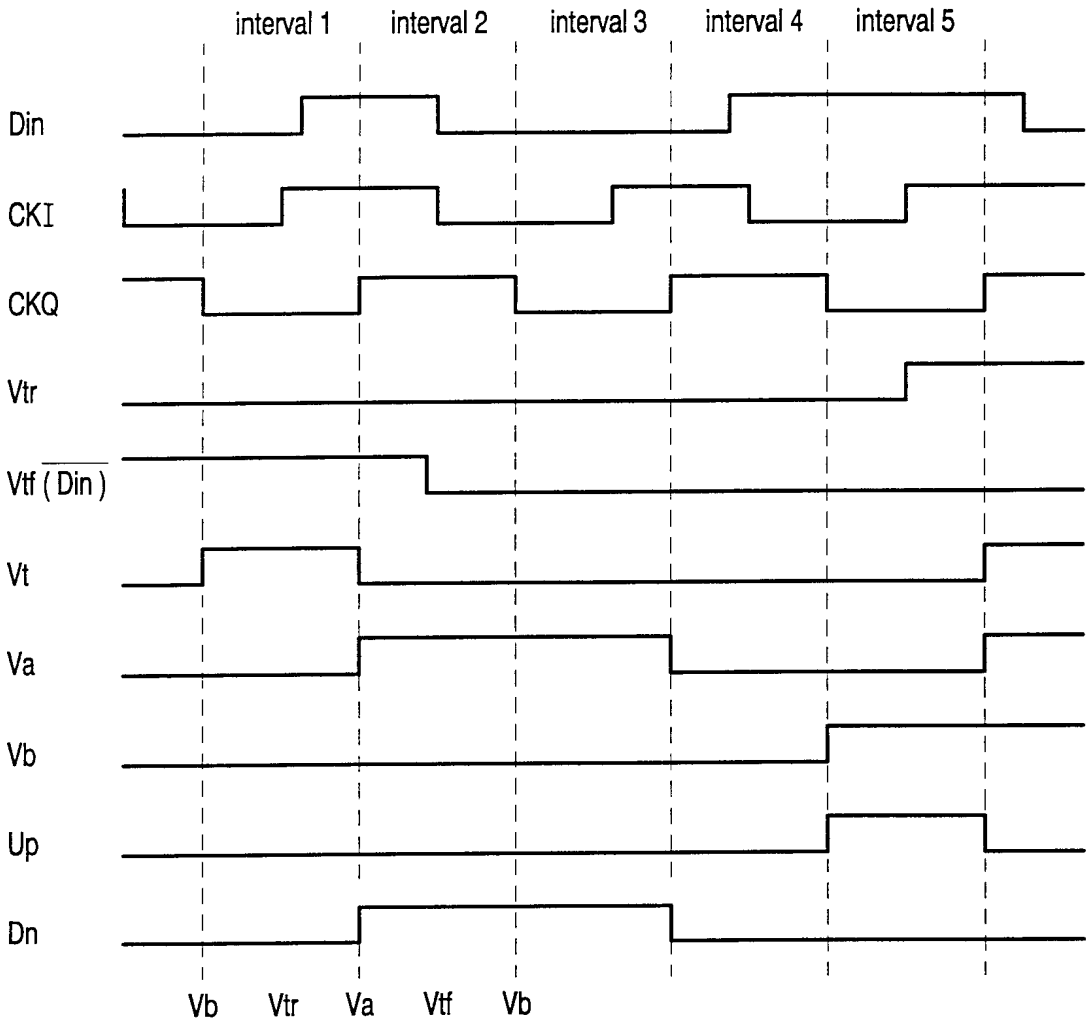
interval 1
interval 2
interval 3
interval 4
interval 5
Din
CKI
CKQ
Vtr
Vtf (Din)
Vt
Va
Vb
Up
Dn
Vb
Vtr
Va
Vtf
Vb

FIG. 3

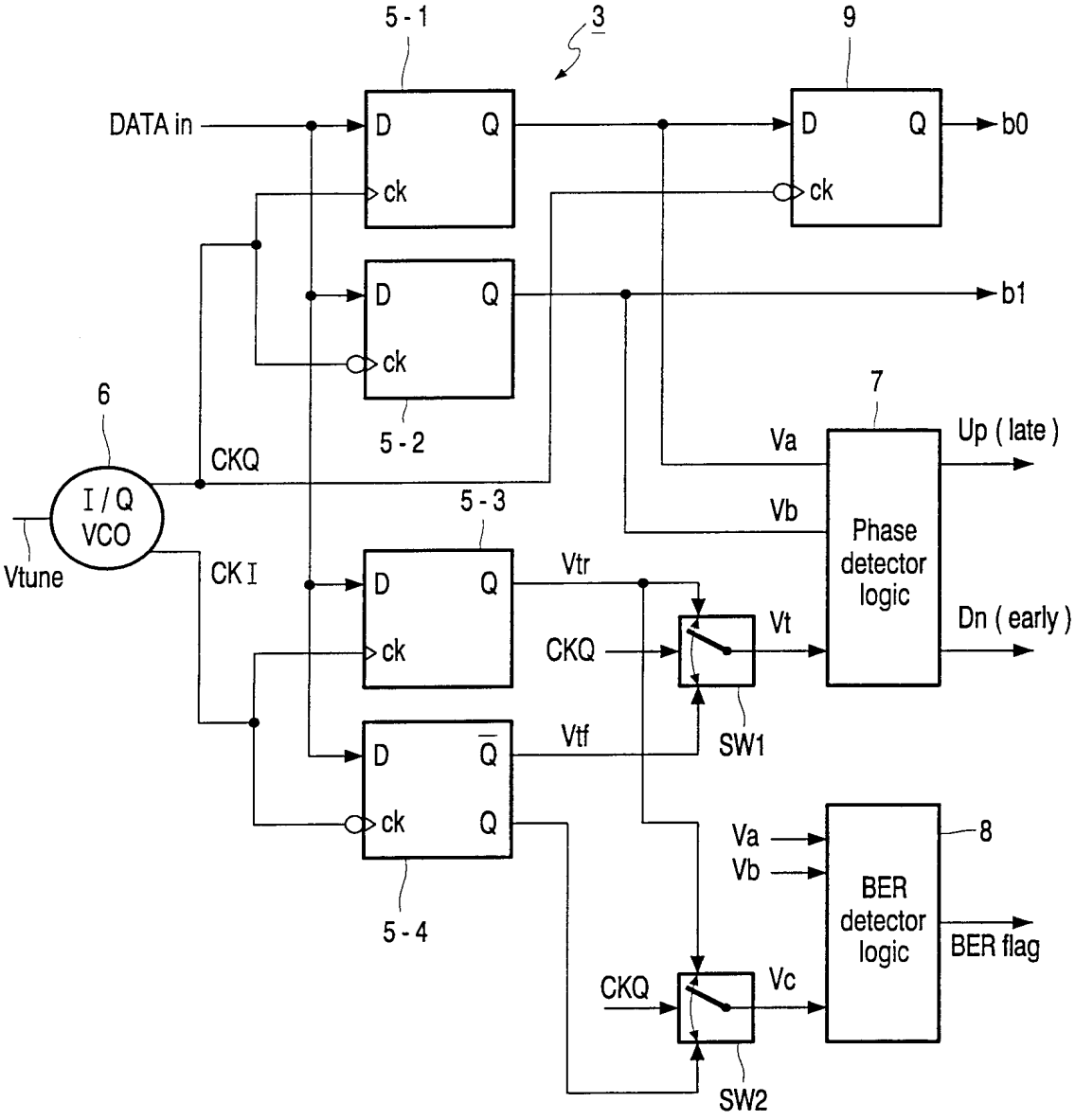

FIG. 4

Va	Vb	Vt	Up (late)	Dn (early)
0	0	X	0	0
1	1	X	0	0
0	1	0	1	0
0	1	1	0	1
1	0	0	0	1
1	0	1	1	0

FIG. 6

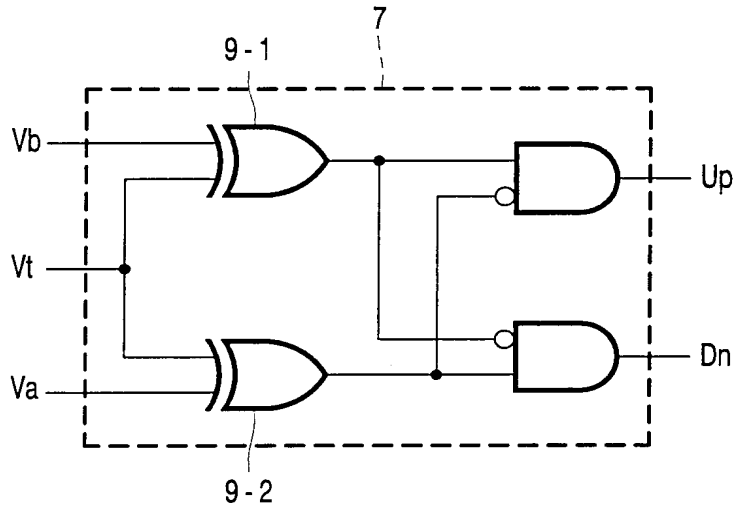

FIG. 5a

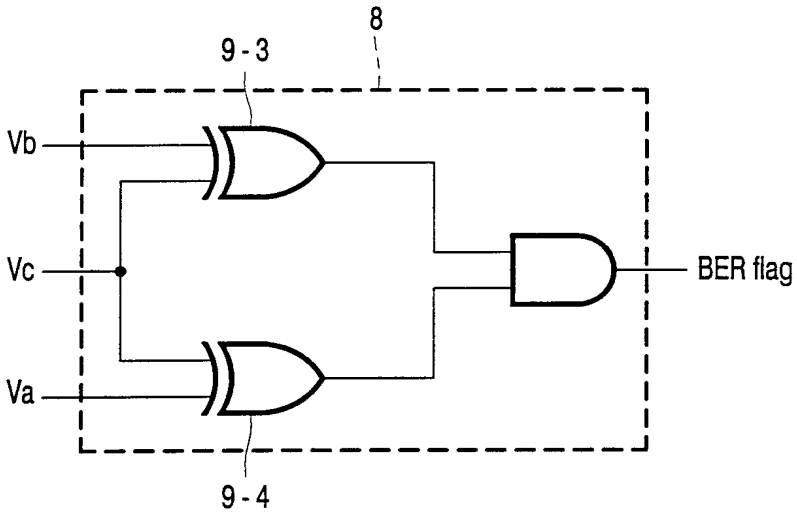

FIG. 5b

INTERNATIONAL SEARCH REPORT

Inter ional Application No
PCT/EP 01/02157

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H03L7/089 H03L7/091 H04L7/033

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H03L H04L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, INSPEC, COMPENDEX

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	DE 197 17 586 C (SIEMENS AG) 27 August 1998 (1998-08-27) column 1, line 54 -column 3, line 40; figures	1-3,8,9
A	---	7
X	RAU M ET AL: "CLOCK/DATA RECOVERY PLL USING HALF-FREQUENCY CLOCK" IEEE JOURNAL OF SOLID-STATE CIRCUITS,US,IEEE INC. NEW YORK, vol. 32, no. 7, 1 July 1997 (1997-07-01), pages 1156-1159, XP000729379 ISSN: 0018-9200 page 1156, column 1, line 1 -page 1157, column 2, last line; figures 2-5	1-3,8,9

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[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

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"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
5 July 2001	12/07/2001

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Balbinot, H

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Form PCT/ISA/210 (second sheet) (July 1992)

INTERNATIONAL SEARCH REPORT

Inte. .ional Application No
PCT/EP 01/02157

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document. with indication.where appropriate. of the relevant passages	Relevant to claim No.
X	RAU ET AL.: "1 Gb/s clcok recovery PLL in 0.5 mu m CMOS" PROCEEDINGS OF THE 22ND EUROPEAN SOLID-STATE CIRCUITS CONFERENCE, PROCEEDINGS OF ESSCIRC '96, 1996, pages 68-71, XP001010891 page 68 -page 69; figures 1-3 ---	1-3,8,9
P,X	US 6 075 416 A (DALMIA KAMAL) 13 June 2000 (2000-06-13) column 2, line 16 -column 4, line 30; figures 2-4	1,2,8,9
P,A	-----	3,4

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INTERNATIONAL SEARCH REPORT

Inter ..ional Application No
PCT/EP 01/02157

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DE 19717586 C	27-08-1998	NONE	
US 6075416 A	13-06-2000	NONE	